EE 3300 Laboratory 6
Resistors, Bonding Pads, and Pad Frames
Fall 2024

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Objective

The objective of this experiment is to investigate the design and layout of resistors, the basic bonding pads that comprise a pad frame, and diodes. This knowledge will then be used to design a bonding pad + ESD protection circuit using components from the tsmc18rf library.

Checkpoints

The checkpoints for this lab are as follows:

1. $10k\Omega$ Resistor Layout
2. Bonding Pad Layout (w/ Measurements) + DRC
3. Diode Layout + DRC
4. Bondpad Circuit, Layout, and DRC + LVS
5. Transient Analysis Proving ESD Class

As with all future labs, these checkpoints must be shown to a lab TA before you submit your lab report. You should include these checkpoints in your lab report.

Part 1: Layout of a Resistor

A resistor can be created using almost any layer available in the process. For example, in the tsmc18rf process, a rectangular, P^+ doped poly resistor can be created by drawing a rectangular poly region encompassed by a PIMP rectangle with terminals at its ends as shown in Figure 1 (top). The value of this resistor will be the product of the sheet resistance times the number of squares (Note: A corner counts as 0.55 squares). The resistor is often shaped to reduce the overall area, often making a U shape or serpentine for larger resistances.

Since a layout pattern with contacts on two ends can be used for either an interconnect or for a resistor, and since the same physical devices are used for both, the CAD tools have no way of determining strictly from the layout of the resistor what is intended to be a resistor that appears in a circuit schematic and what is intended to be an interconnect. To allow the CAD tools to correctly recognize the regions that correspond to resistors in a circuit schematic, special layers are used to denote areas in the layout that correspond to a resistor in the schematic (typically these layers have a name like RXDUMMY - drawingY where X and Y are variables that determine different types of resistors). These layers mean nothing physically. They do not alter how the die is manufactured. They are simply notational devices so that LVS can run properly. In Figure 1 (bottom), the dummy layer is shown for the resistor layout of Figure 1 (top).

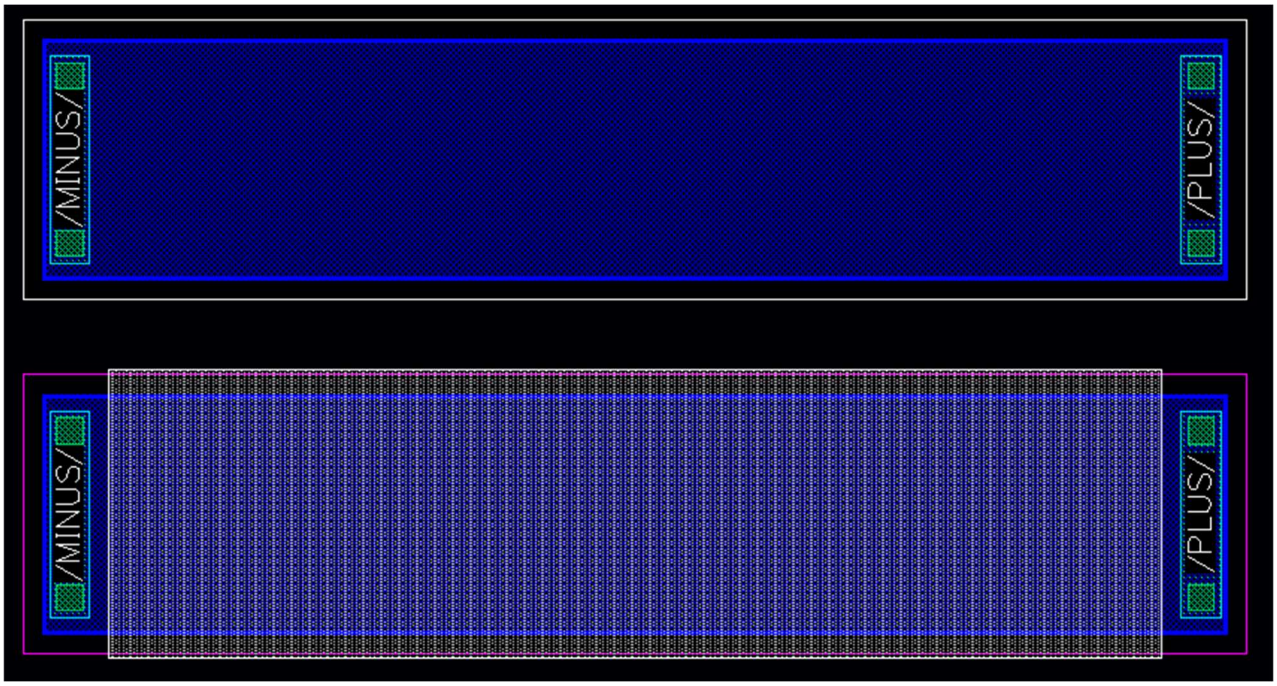

Figure 1: Top: P^+ Doped Poly1 Resistor in tscm18rf Process, Bottom: Same Resistor as Top with Dummy Layer Shown

Part 1.1 Create a Resistor Layout

For this part of the lab, you will create a P+ doped Poly 1 resistor layout similar to that shown in Figure 1. This is a resistor made out of Poly 1 that is then doped (similar to how the MOSFET diffusions are doped). Make a P+ Poly1 resistor (using the direction given below) with a resistance of 10 kΩ (+/- 1%). The sheet resistance of P+ doped Poly1 is 311 ohms/square.

You are encouraged to experiment with ways of shaping the resistor to maximize the resistance to area ratio. For example, a serpentine layout could be used like that shown in Figure 2.

You need to use 4 elements to make the resistor: Poly1 resistor routing, RPDUMMY (drawing) rectangle, Poly1 to Metal 1 vias, and a PIMP rectangle. The main part of the resistor is made of Poly1. The RPDUMMY – drawing layer is used to denote what Poly1 makes up the resistor. You need to make sure that you have the correct number of squares made by the Poly1 and covered in an RPDUMMY – drawing rectangle. Your Poly1 can stick out a bit to add vias (see Figure 1). Add vias to either end of your resistor to form the terminals. Lastly, cover the entire resistor layout with a PIMP rectangle. PIMP tells the CAD tools that the Poly1 within its boundaries will be implanted with P type impurities.

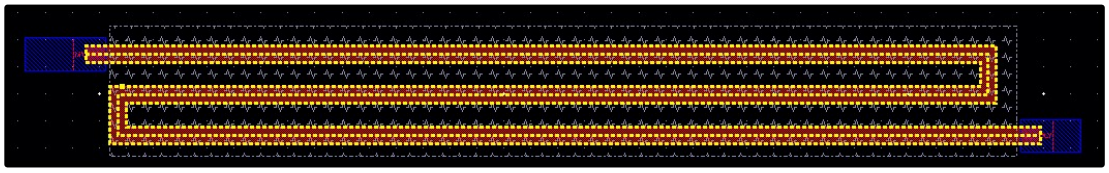

Figure 2: Serpentine Resistor Layout (From the ON 0.5u Process)

Make the resistor layout and ensure that it passes DRC. Show your layout, correct DRC results, and calculations that show that the resistor is 10 kΩ (+/- 1%) to your TA for the checkpoint.

Part 2: Introduction to Bonding Pads

A bonding pad is used as part of the connection of the circuit on a die to a pin on a package. One side of a wire (often gold) connects to the bonding pad while the other side connects to the corresponding pin on a package. This interconnecting wire is called a "bonding wire". Although only the top metal layer (Metal 5 for the tsmc18rf process) is used for the connection with the bonding wire, the bonding pad is typically made of all available metal layers stacked on top of each other and interconnected through vias. This arrangement allows connection from the core of the chip to the pad and, in turn, the outside world using any metal.

Figures 3 and 4 show how a silicon die would be placed in a package with its bondpads connected to the package pins through gold wires.

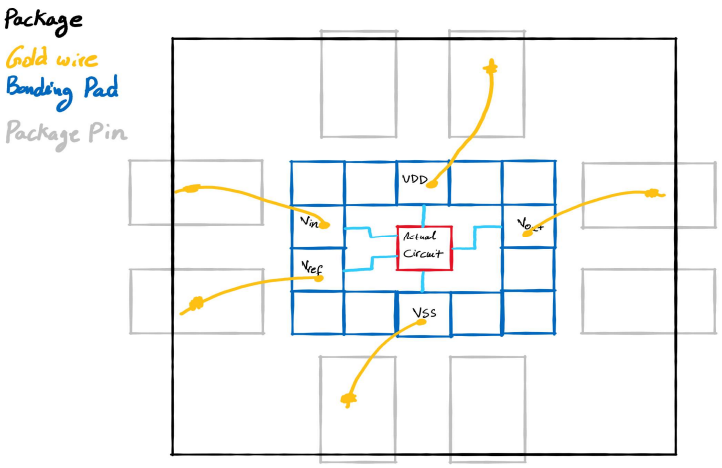

Figure 3: Silicon Die with Circuit in the Middle and Bondpads Around the Outside Connected to a Package (Top View)

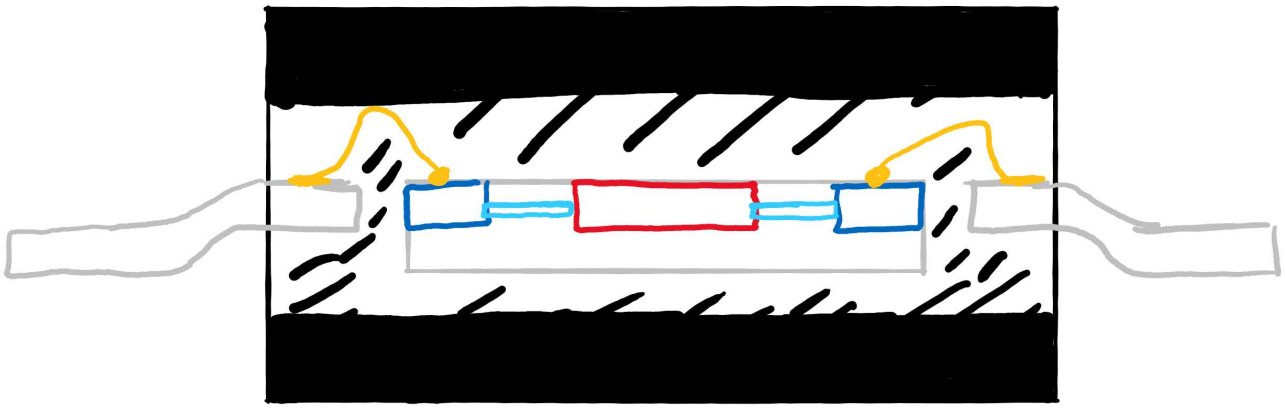

Figure 4: Silicon Die with Circuit in the Middle and Bondpads Around the Outside Connected to a Package (Side View)

The last major processing step in the manufacturing of a wafer is adding the "passivation" layer. The passivation layer is an insulating layer that covers the entire chip to protect circuits from environmental contamination or minor damage on the surface. Since the bonding pads need to be accessible for electrical connection to the chip package, this top passivation layer must be removed from the areas where the bonding pads reside.

When making bondpads, it is important to mark that the passivation layer must be removed above the bondpad. In the tsmc18rf process, the "PAD" layer is used for this purpose. Anywhere there is PAD layer in the layout, the passivation layer will be removed during manufacturing.

Part 2.1: Create the Layout of a Bonding Pad

Create a bonding pad comprised of stacked layers of metal 1-5 with a pad opening in the passivation layer. Use stacked vias (stacking of vias is allowed in the tsmc18rf process) to interconnect these metal layers. To minimize the resistance in the interconnections of these metal layers, use near the maximum possible number of vias, by creating multiple rows and columns, when connecting adjacent metal layers. The passivation opening should be 60µm x 60µm. The opening must lie completely within the pad and the pad (metal) should extend at least 8µm beyond the edges of the passivation opening (typically this is given by a design rule but tsmc18rf is a fake process and does not have a clear design rule – so, for our purposes, we are choosing 8µm as the rule).

Show your layout and successful DRC results to your TA. Also show that you used many vias and that the metal extends beyond the PAD rectangle by 8um. These are the deliverables for the second checkpoint.

Hint: You can cover the entire surface of a pad with vias efficiently (and create the metal layers while you are at it). Begin creating a via like normal, but then, in the options, select "Stack" for the mode, Metal 1 as the start layer, Metal 5 as the end layer, and set the number of rows and columns to create the area you need. This will create a rectangle for each metal layer and an array of vias between each metal layer.

Part 3: Layout of a Diode

In the n-well bulk CMOS process, diodes can be created in two ways: one is with a p+ diffusion in an n-well and the other is with a n+ diffusion in the p-substrate. These two ways of creating a diode are depicted in Figure 2. Though this represents two ways to create a diode, the n+/p-substrate diode has very limited applications since its anode is inherently connected to the substrate. Even the p+/n-well diode has some limitations since there is actually a p-sub/n-well diode also present (not shown in Figure 5). The node labels in this figure denote the contacts to the anodes and cathodes of the diodes. For example, the cathode for the p+/n-well diode on the right is actually the n-well or more precisely the n-well region immediately adjacent to the p+ diffusion.

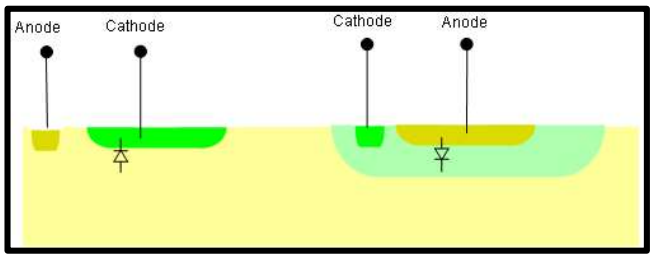

Figure 5:Two Ways to Make Diode in n-well CMOS Process; n+/p-substrate on left and p+/n-well on right

For this lab, we will use the p+/n-well diodes and layout each diode in its own n-well, as in Figure 5.
The area factor, A, in the diode equation (1) is the area of the intersection of the diffused regions that form the anode and the cathode. In this layout, the cathode surrounds the anode so the area factor, A, is the area of the anode which is formed with the p+ implanted region. Figure 6 shows a p+/n-well diode layout in the tsmc18rf pdk. Figure 7 shows the layer definitions for the layout. Note that the diode is surrounded by a rectangle of layer DIODUMMY. The DIODUMMY layer tells Cadence that the layout within its boundaries forms a diode.

$$I_D = I_S\left(e^{\frac{V_D}{V_t}} - 1\right) = J_S A(e^{\frac{V_D}{V_t}} - 1) \qquad (1)$$

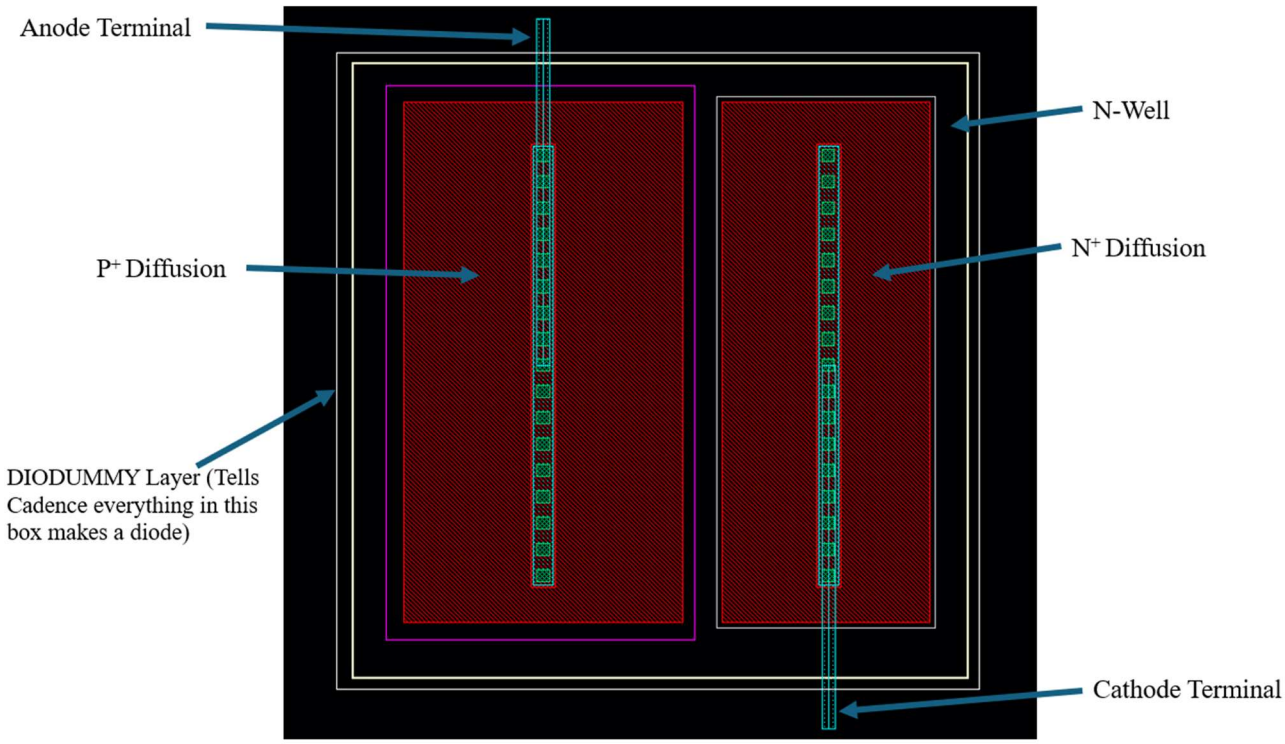

Figure 6: Simple P+/N-Well Diode Layout Made in the tsmc18rf PDK

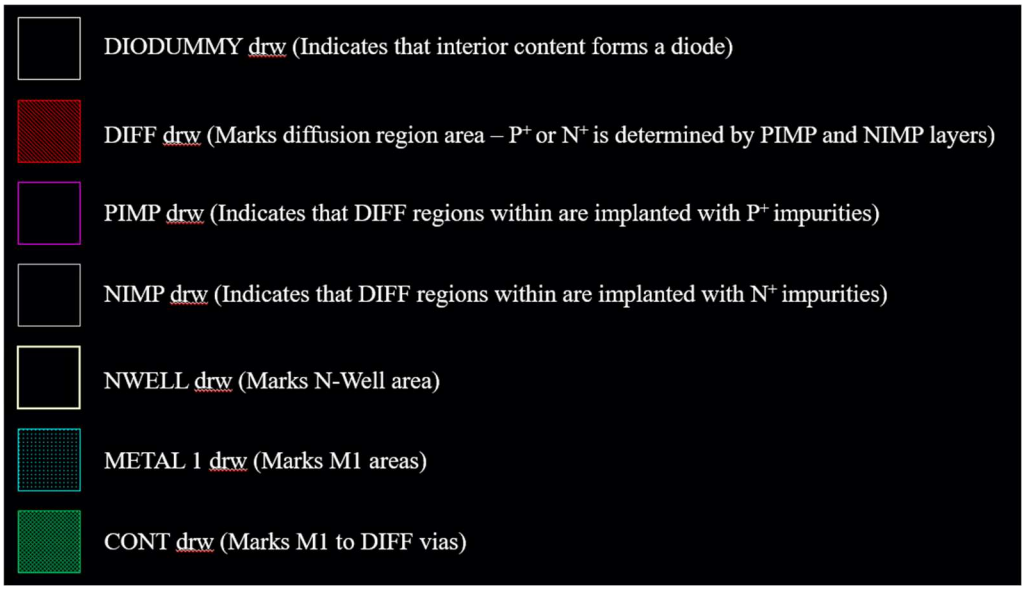

Figure 7: Layer Definitions for the Diode Layout Shown in Figure 4

Part 3.1 Create a Diode Layout

Create a layout for a p+/n-well diode. Make the diode a square (square N-Well) and make the Anode to be much larger than the Cathode (at least 4x). An example (does not meet the specs above) layout is shown in Figure 6. Make sure the layout passes DRC.

Show your layout and successful DRC results to your TA for the third checkpoint.

Part 4: ESD Protection Circuitry

Electrostatic discharge (ESD) is a rapid flow of current typically associated with breakdown of air or other gasses. This breakdown is associated with the rapid formation of a plasma. Lightning is one example of electrostatic discharge. If you've ever dragged your feet on carpet so you can shock someone with the tip of your finger, you've created an electrostatic discharge. If the discharge path includes a path through an integrated circuit, the sudden surge of electrons associated with ESD can damage or destroy the devices in a circuit. Simply touching an integrated circuit can cause an ESD event if a person is sufficiently charged. The person could become charged by walking across a carpet or even a dry floor in a low humidity environment.

Damage in the integrated circuit occurs because the ESD currents create short, yet very large voltage pulses breakdown the transistors and devices and cause the integrated circuit to fail. In manufacturing environments, there are ways to mitigate the ESD risk by using protocols that may include an ESD smock/wristband/mat, a humidity-controlled environment, and/or ESD safe tools. However, this mitigation does not exist in the real world, where our circuits will operate. Therefore, we need to build ESD protection into our integrated circuits so they are protected from ESD damage.

Designing ESD protection circuitry is a difficult task and is not rigorously taught in educational settings. Much of the ESD protection circuitry knowledge resides in companies. Often, ESD protection circuitry is designed by experienced, specialized engineers and provided to the circuit designers (you).

For the purpose of this lab, you are going to create the simple ESD protection circuit shown in Figure 8. The simple circuit discussed in this experiment will provide a reasonable level of ESD protection though an actual production circuit will probably have a much better ESD protection architecture. In this ESD protection circuit the resistor R_{PROT} is to be made using a poly resistor with a ***value of 50 ohms***.

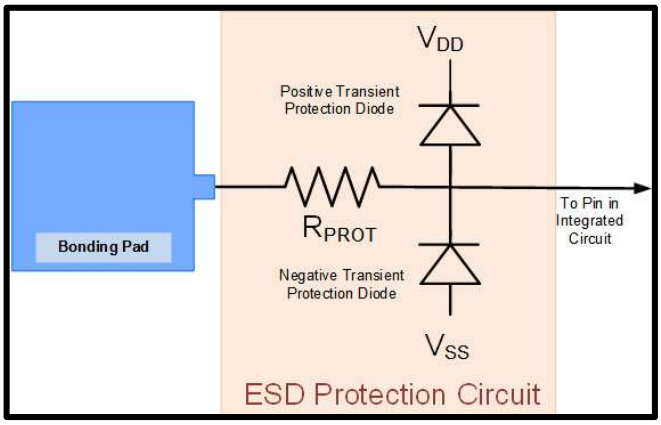

Figure 8: ESD Protection Circuit Schematic

If an ESD event occurs on a bonding pad without ESD protection, the corresponding voltage on the bonding pad can be very large and will propagate directly into the integrated circuit thereby damaging or destroying the IC. But with the ESD protection circuit shown, the actual voltage that gets into the circuit will be limited to about 0.7V above V_{DD} or to about 0.7V below V_{SS}. The excess voltage incident on the bonding pad will be impressed across the resistor R_{PROT}. Many types of resistors can support a large voltage for a short period of time without damaging the resistor. And many diodes can support a large current flow for a short period of time without damaging the diode.

Every pin on the integrated circuit will have a pad protection circuit. Depending upon whether the pin is an input, an output, or a supply voltage, the protection circuit will vary. These variations could be in the size of

the resistor, in the size of the diodes, or in some other modifications to the protection circuitry. Pad protection circuits are generally included in a library and the designer simply selects the protection circuit that corresponds to the functionality of each node.

Part 4.1 Create a Pad Protection Schematic, Symbol, and Layout

Create a new schematic (call it bondingPadWithESD or something similar) and recreate the schematic of the ESD protection circuit (the Bonding Pad is just an input pin in this schematic). This schematic will be used for LVS later. Use either the "diodep3v" diode (these are equivalent to the diode you built earlier) from the tsmc18rf pdk and the "rphpoly", "rphripoly", "rplpoly", "rnhpoly", or "rnlpoly" resistor from the tsmc18pdk. Think about making the diodes pretty large (total area of ¼ the area of your bondpad layout from earlier).

Your schematic should have 4 pins – VDD, VSS, PAD_IN, and PAD_OUT (or similar names). Also make a symbol for your bondpad + ESD protection schematic.

Make the layout for the bondpad and ESD protection circuit. To do so, use the generate from source option to import the resistor, diodes, and pins (like we did in the previous lab). Also manually import your bondpad by pressing I, then selecting lablib for the library, and your bondpad cell as the cell. Place the PAD_IN pin on the bondpad and connect everything else as needed.

Run DRC and LVS for your design and make sure they are successful. Show your schematic, layout, and DRC + LVS results to your TA for the fourth checkpoint.

Part 5: Testing the ESD Protection Circuit

Now that you have made your bondpad + ESD protection circuit, it is time to test how well it works. To test the circuit, a model is needed which replicates the ESD stress that would be applied to the circuit in real life. Several models are available. The model we will use for this lab is called the Human Body Model.

Part 5.1: Human Body Model

The human body model is an electrical equivalent of a human touching a circuit to induce static discharge. It is modeled as a 100pF capacitor discharging through a 1500 ohm resistor in series to the device under test (DUT). The human body model (HBM) is shown in Figure 9. Devices are qualified into different classes depending upon how much voltage they can handle from this configuration. The different classes can be found in 11.

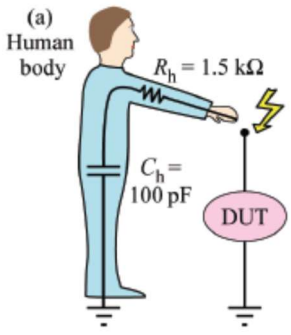

Figure 9: HBM

Create a new schematic and call it **HBM_TB**. Add the human body model (an ideal capacitor and resistor from analoglib) and your protection circuitry. Remember to hook up Vss and Vdd (use VSS = 0V and VDD =

3.3V). Use a 1pF capacitor (analoglib) as the load connected to the PAD_OUT pin. Set the starting voltage of the charged capacitor using the 'Initial Conditions' query in the properties of the 100pF capacitor. Set the starting voltage of the 1pF load capacitor to 0V.

Before simulating your test circuit, you must include the Spectre model libraries for the resistor and diodes. To do this, open ADE Explorer, create a test for your schematic, and go to Setup -> Model Libraries and a popup will appear like Figure 10.

Click on “click here to add model file”. Add the following line:
/remote/cadencelib/tsmc018/models/spectre/cor_dio3.scs

Click in the section dropdown and select “dio3”.

Repeat for the following line and section: /remote/cadencelib/tsmc018/models/spectre/cor_res.scs (tt_res section)

Your setup should now look like Figure 10.

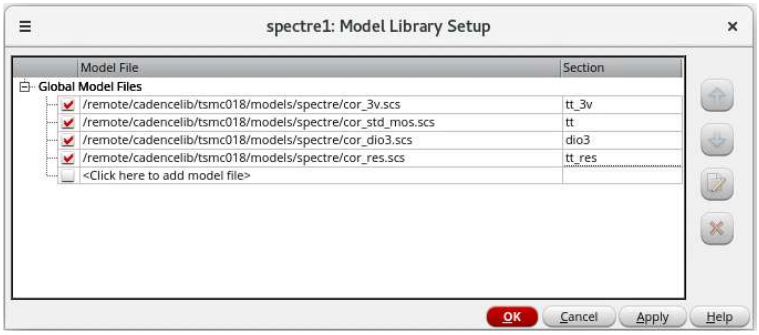

Figure 10: Including Model Libraries

Run the circuit for a variety of starting voltages and see how the protection circuitry works. If we specify Vdd = 3.3V and any voltage above 5V destroys the circuitry (a capacitor in this simulation), to what class of devices would this belong? How could you improve the protection of the circuit? The classes are shown in Figure 11.

Report the class of the ESD protection to your TA and show them your testbench for checkpoint 5.

Class	ESD withstand voltage, V_w
0	0 ~ 250 V
1A	250 ~ 500 V
1B	500 ~ 1000 V
1C	1000 ~ 2000 V
2	2000 ~ 4000 V
3A	4000 ~ 8000 V
3B	> 8000 V

Figure 11: HBM Classifications